



EI Labs India Pvt. Ltd.

Embedded Devices



LinSeedV2

Product Technical Information

Doc Name : LinV2DS version 1.0

Dated : Jan 2008

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NOTE

The LinSeed series of SoftChips is a tight system integration of third party semiconductor devices. EILABS India has tried to provide accurate information to the best of its knowledge. However, no responsibility is assumed for its use and such information is provided “as is” without any warranty of any kind, implied or otherwise. The device specification is subject to change as per the continuous improvement policy of EILABS India.

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1.0 OVERVIEW.

LinSeedV2 is a state of the art, 60 pin Integrated SoftChip and is the second in a series of LinSeed modules. The SoftChip concept encapsulates the hardware completely from a user perspective and provides them with a very high level software API for configuration, control and data processing. The LinSeedV2 is a 32 bit processing module with standard Linux API for the user. The hardware details are required only to the extent of the external interfaces on the user board for the purposes of further system development. Traditional SoC programming information like internal registers, peripherals etc are not required for the system designer of LinSeedV2. All peripherals are accessed through appropriate Linux drivers. This fundamentally is a big value proposition of the offering.

LinSeedV2 is tight system integration on a 10 layer PCB of the following

- ARM 9 processor running at 180 MHz
- Built-in 16MB Flash and 32MB SDRAM.
- Linux kernel ported into Flash and Ready to run when powered up.

The entire circuit design is enclosed in a metal can, which acts as the EMI shield. New applications with user defined I/O up and running in less than a month by plugging in the LinSeedV2 module in user- defined 2 / 4 layer PCB.

Linseed supports the following Peripherals/ GPIO's.

a.	USB Host:	2 ports.
b.	USB Device:	1 port.
c.	Serial Synchronous Communications:	3 ports
d.	I2C I/F:	1 port.
e.	Full function UART:	1 port.
f.	Half function UART:	1 port.
g.	Debug.	1 port.
h.	RTC	
i.	GPI/O's	9
j.	Ethernet.	100 Megabits per sec.
k.	SPI I/F:	3 ports.

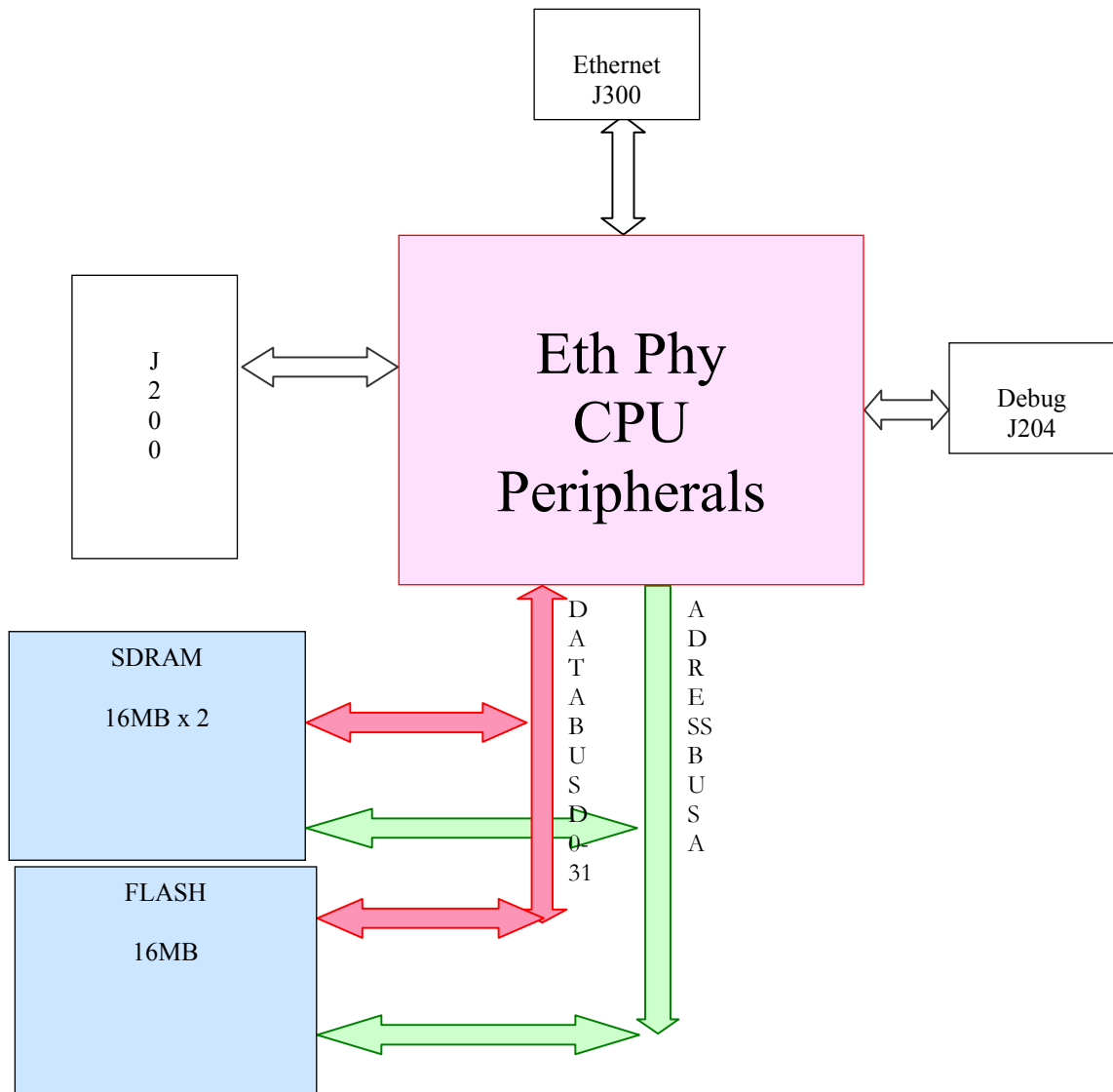
1. 3.3V D.C. This is used to power the External Bus I/O Lines and the Peripheral I/O lines.
2. **The 1.8VDC required to power the core of Linseed V2 is generated on board internally and is not available to the user for external use.**

BLOCK DIAGRAM

The block schematic of linseed V2, 60 pin soft chip(J200) with 1.27mm pitch, connectors of 1X30, placed as DIP connector is as shown below

Additionally, it has two other connectors:

- a. J300(2X3=6 pins with 1.27mm pitch) for Ethernet.
- b. J204(1X3=3 pins with 1.27mm pitch) for Debug port.



MEMORY MAP

Memory	Memory range
Flash	0x1000 0000 - 0x10FF FFFF
SDRAM	0x2000 0000 - 0x21FF FFFF

2.0 LinSeed Functional Pinout

VCC33	1	POWER	EIL LinSeed	GND	60	GND
VCC33	2			GND	59	GND
VCC33	3			IRQ	58	IRQ0
VCC33	4				57	IRQ1(3)
RF	15	SSC (AUDIO)		GPIO	53	NA
RK	6				42	GPIO_1
RD	5				40	GPIO_2
TD	17				51	GPIO_3
TK	16				43	GPIO_4
TF	18				52	GPIO_5
RTS	13				55	GPIO_6
DSR	12	56			GPIO_7	
CTS	14	54			NA	
DCD	11	41			NA	
RDX	9	44			GPIO_10	
TDX	7	50		GPIO_11		
DTR	10	UART0		SPI	47	SPICK
RI	8				38	MISO
RX0	24				46	MOSI
TX0	23				48	SPI_CS0
TWCK	27	45	SPI_CS1			
TWD	28	49	SPI_CS2			
USB_DP_PUP	25	USB DEVICE	GPIO	39	GPIO_12	
USB_CNx	26		NRST	37	NRST	
DDP	19		GND	36	GND	
DDM	20			35	GND	
HDPB	29	34		GND		
HDMB	30	USB HOST2	33	GND		
HDPB	21		CORE POWER	32	VCC18 *	
HDMA	22			31	VCC18 *	

NA: STANDS FOR NOT AVAILABLE TO USER.

* Generated internally on board, and is meant only for driving the core of the Arm 9 Processor, and is not meant/ available for external user Interface.

3.0 Pin Details.

External Connector J200: 2 x 1.27mm berg connector male 1x 30.

PIN. NO.	PIN NAME	FUNCTION	TYPE OF SIGNAL	SIGNAL LEVEL		
				MIN.	TYPICAL	MAX.
01.	VCC33	POWER FOR PERIPHERALS & I/O.	IN	3V.	3.3V.	3.6V.
02.	VCC33	POWER FOR PERIPHERALS & I/O.	IN	3V.	3.3V.	3.6V.
03.	VCC33	POWER FOR PERIPHERALS & I/O.	IN	3V.	3.3V.	3.6V.
04.	VCC33	POWER FOR PERIPHERALS & I/O.	IN	3V.	3.3V.	3.6V.
05.	RD	SSC RCR DATA.	IN		3.3V.	
06.	RK	SSC RCR CLOCK.	IO		3.3V.	
07.	TDX	FF UART TX DATA.	OUT		3.3V.	
08.	RI	FF UART RING INDICATOR.	IN		3.3V.	
09.	RDX	FF UART RX DATA.	IN		3.3V.	
10.	DTR	FF UART DTR.	OUT		3.3V.	
11.	DCD	FF UART DATACARRIER DETECT.	IN		3.3V.	
12.	DSR	FF UART DATASET READY.	IN		3.3V.	
13.	RTS	FF UART RTS.	OUT		3.3V.	
14.	CTS	FF UART CLEAR TO SEND.	IN		3.3V.	
15.	RF	SSC RECEIVER FRAME SYNCHRO.	IO		3.3V.	
16.	TK	SSC TRANSMITTER CLOCK.	IO		3.3V.	
17.	TD	SSC TRANSMITTER DATA.	OUT		3.3V.	
18.	TF	SSC TRANSMITTER FRAME.	IO		3.3V.	
19.	DDP	USB DEVICE PORT DATA +.			ANALOG	
20.	DDM	USB DEVICE PORT DATA -.			ANALOG	
21.	HDPA	USB HOST PORT A DATA+.			ANALOG	
22.	HDMA	USB HOST PORT A DATA -.			ANALOG	
23.	TX0	HALF FUNCTION UART TRANSMITTER.	OUT		3.3V.	
24.	RX0	HALF FUNCTION UART RECEIVER.	IN		3.3V.	
25.	USB DP PUP	PULL UP FOR USB DEVICE.	OUT			

26.	USB CNX	SIGNAL TO CHK. WHETHER HOST IS CONNECTED.	IN			
27.	TWCK	I2C CLOCK.	IO		3.3V.	
28.	TWD	I2C DATA.	IO		3.3V.	
29.	HDPB	USB HOST PORT B DATA+.			ANALOG	
30.	HDMB	USB HOST PORT B DATA -.			ANALOG	
31.	VCC18 *	ON BOARD GENERATED POWER FOR CORE.	FOR INTERNAL USE ONLY.	1.65V.	1.8V.	1.9V.
32.	VCC18 *	ON BOARD GENERATED POWER FOR CORE.	FOR INTERNAL USE ONLY.	1.65V.	1.8V.	1.9V.
33.	GND.	LOGIC GROUND.				
34.	GND	LOGIC GROUND.				
35.	GND	LOGIC GROUND.				
36.	GND	LOGIC GROUND.				
37.	NRST	RESET.	IN			
38.	MISO	SPI MASTER IN SLAVE OUT	IO		3.3V	
39.	GPIO_12	GPIO 12.	IO		3.3V	
40.	GPIO_2	GPIO 02.	IO		3.3V.	
41.	NA	NOT AVAILABLE TO USER				
42.	GPIO_1	GPIO 01.	IO		3.3V.	
43.	GPIO_4	GPIO 04.	IO		3.3V.	
44.	GPIO_10	GPIO 10.	IO		3.3V.	
45.	SPI_CS1	SPI CHIP SELECT 1	OUT		3.3V.	
46.	MOSI	SPI MASTER OUT SLAVE IN.	IO		3.3V.	
47.	SPICK	SPI CLOCK.	IO		3.3V.	
48.	SPI_CS0	SPI CHIPSELECT 0.	IO		3.3V.	
49.	SPI_CS2	SPI CHIP SELECT2.	OUT		3.3V.	
50.	GPIO_11.	GPIO 11.	IO		3.3V.	
51.	GPIO_3	GPIO 03.	IO		3.3V.	
52.	GPIO_5	GPIO 05.	IO		3.3V.	
53.	NA	NOT AVAILABLE TO USER				
54.	NA	NOT AVAILABLE TO USER				
55.	GPIO_6	GPIO 06.	IO		3.3V	
56.	GPIO_7	GPIO 07.	IO		3.3V.	
57.	IRQ1	INTERRUPT 1	IN			
58.	IRQ0	INTERRUPT 0	IN			
59.	GND.	LOGIC GROUND	LOGIC GROUND			
60.	GND.	LOGIC GROUND	LOGIC GROUND			

NOTE

The Carrier board should cater to the following:

- a. A stable, 3.3V D.C supply to power the peripherals, memory etc.
- b. At power on, the Reset pin NRST/, Pin37 of Linseed should be connected to a power on reset circuit, which will keep the NRST/ line low for about 1000 milli seconds, to allow all the clocks, including the slow clock on the LinSeed module to stabilize before the program execution can begin.

J204. Debug Connector: (1 x 1.27mm berg connector male 1 x 3.)

Debug UART signals are connected to this connector. All the signals are at CMOS level.

Pin No	Name	Pin Description
1	DBGU_TXD	Debug Transmit Data
2	GND	Ground
3	DBGU_RXD	Debug Receive Data

J300. Ethernet Connector. (1 x 1.27mm berg connector male 2 x 3).

Ethernet signals are connected to this connector. All the signals are at CMOS level.

Pin No	Name	Pin Description
1	LED_LINK	Link LED
2	LED_ACT	Activity LED
3	TD+	Transmit Data +ve
4	TD-	Transmit Data -ve
5	RD+	Receive Data +ve
6	RD-	Receive Data -ve

4.0 ENVIRONMENTAL

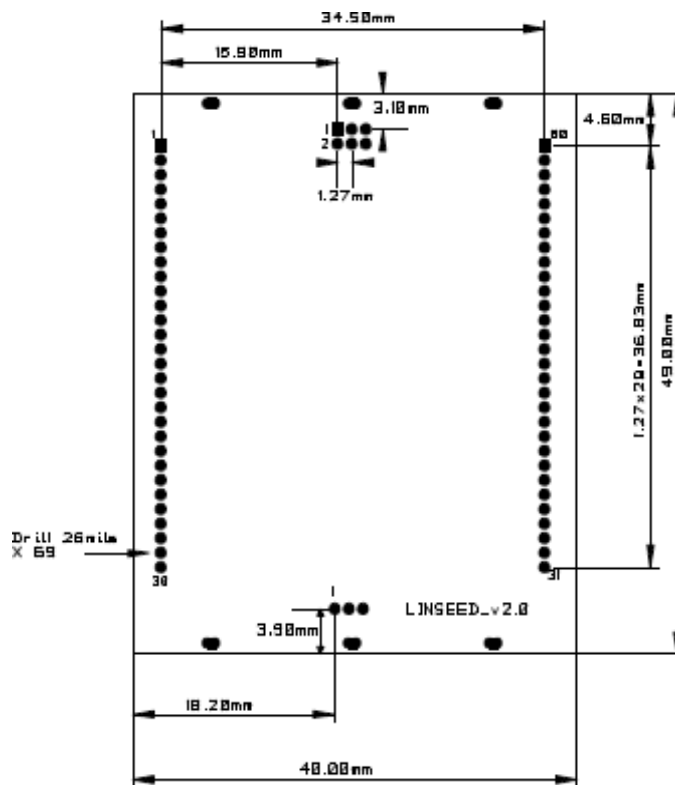
Operating Temperature: -20 Degrees Celsius to + 85 Degrees Celsius (INDUSTRIAL GRADE)

ROHS COMPLIANT.

5.0 MECHANICAL

SIZE : 49.0X 40.0mm

The footprint is provided below



TOP SIDE
LNSEED_v2.0

6.0 EXAMPLE REALIZATION

Check documentation of `LinEvalV2`