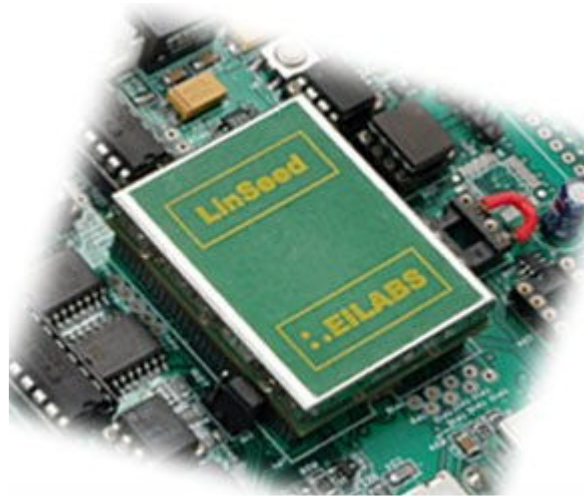




EI Labs India Pvt. Ltd.

Embedded Devices



# LinEval Boardv2

## Product Technical Information

Doc Name : LinEvalV2 version 1.0

Dated : May 2008

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## 1. Overview

LinSeedV2 is a state of the art, 60 pin Integrated SoftChip and is the second in a series of LinSeed modules. The SoftChip concept encapsulates the hardware completely from a user perspective and provides them with a very high level software API for configuration, control and data processing. The LinSeedV2 is a 32 bit processing module with standard Linux API for the user. The hardware details are required only to the extent of the external interfaces on the user board for the purposes of further system development. Traditional SoC programming information like internal registers, peripherals etc are not required for the system designer of LinSeedV2. All peripherals are accessed through appropriate Linux drivers. This fundamentally is a big value proposition of the offering. Please refer the LinSeedV2 product technical information for more information.

LinEvalV2 is designed to be an evaluation platform for the LinSeedV2 module. This board is an evaluation board for LinSeed V2. This is a two layer carrier board on which the LinSeed V2 is plugged in. This board can be used to acquire familiarity and expertise in handling the LinSeed module from the software development perspective, and the peripherals that it can support.

This Evaluation board supports the following peripherals, features and Input/Outputs..

a.	Isolated Digital Inputs	2
b.	Non-Isolated Digital Inputs	4
c.	High Speed Digital Output	4
d.	SPI Interface connector	1
e.	Solid State Relays	2
f.	SPDT Relay	1
g.	USB 2.0 Full Speed Host ports	2
h.	USB 2.0 Full Speed Device Port	1
i.	Half function UART Port	1
j.	Debug Port	1
k.	Full Function UART Port	1
l.	External RTC with Battery Backup	1
m.	Buzzer	1
n.	Software Controlled LED	1
o.	Software Reset Switch	1

### PACKING LIST

- Power Adaptor having a rating of 220VAC to 5VDC with 500mA current output. (OPTIONAL)
- One CD containing User Manual, Kernel and Ramdisk images, Preloaded files, Test Application Source codes, Design Document.

- One Debug Serial Cable with 3 pin Female berg on one side to fit onto the board and a female DB9 connector on the other side to fit to the serial port connector on the PC.

**BLOCK DIAGRAM**

The block schematic of the LinEvalV2 board is given in Figure 1. The actual realization is shown in Figure 2.

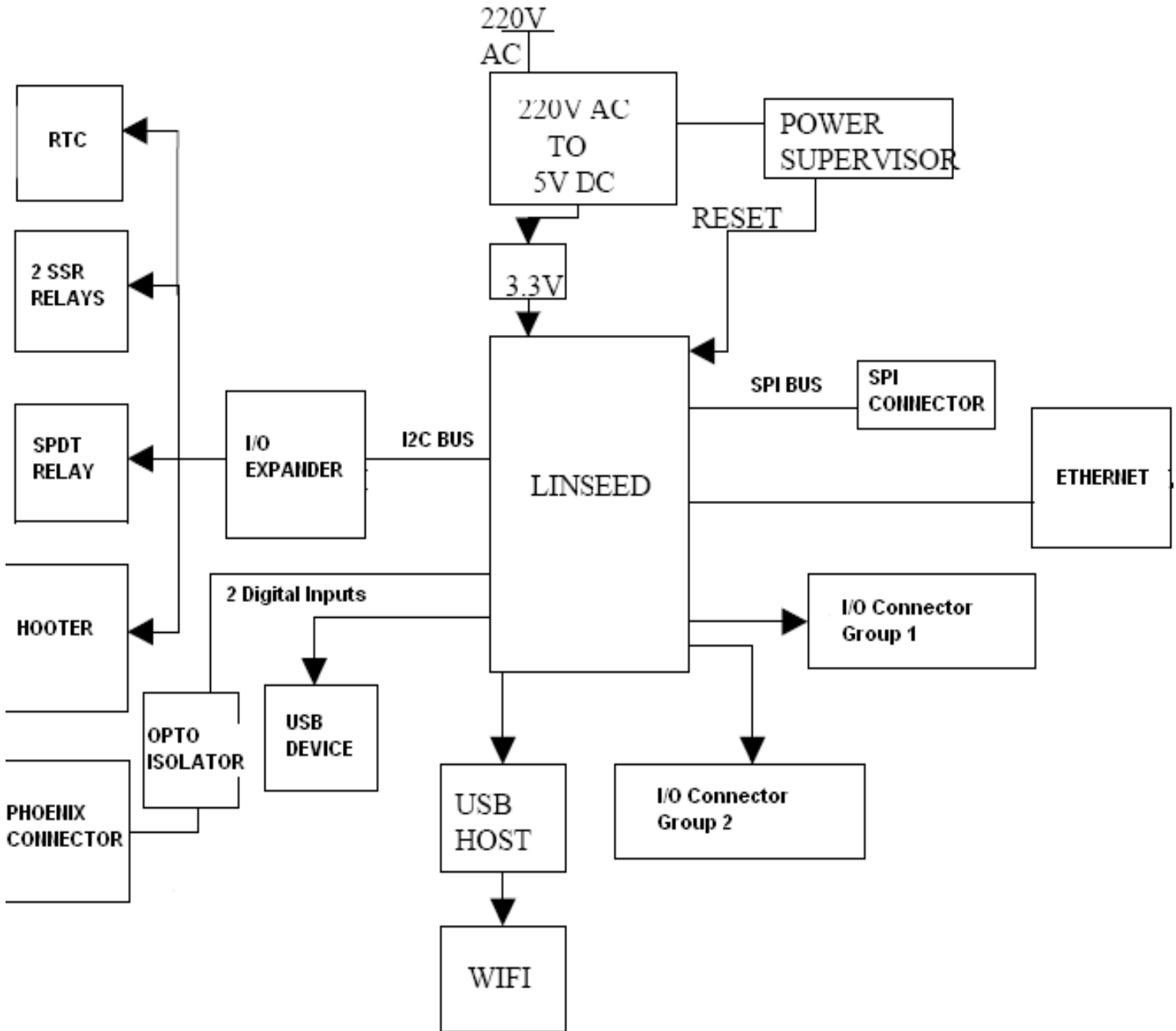
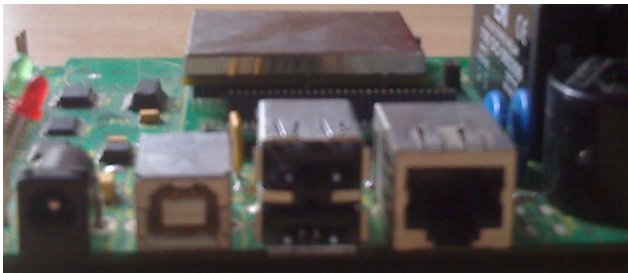


Figure 1 Lin EvalV2 functional block diagram



**Figure 2 Picture of the LinEvalV2board**



## 2. Functional Connector Pin Out

### J100 – Power Connector:

Pin No	Name	Pin Description
1	5V_IN	5 Volts power input
2	GND	Power Ground

### J700 – I/O Group 1 Connector:

5 volt Power supply, half Function UART (TTL level signals), 2 Digital Outputs and 2 Digital Inputs, 1 Interrupt and 3.3 volt power supply pins are terminated onto this connector.

Pin No	Name	Pin Description
1	VCC_5	5 volt power supply
2	VCC_5	5 volt power supply
3	GND	Ground
4	GND	Ground
5	RF1 RDX	Receiver (TTL level)
6	RF1 TDX	Transmitter (TTL level)
7	Digital O/P 0	Digital Output 0
8	Digital O/P 1	Digital Output 1
9	I/O 1 Digital I/P 1	I/O Group 1 Digital Input 1
10	I/O 1 Digital I/P 2	I/O Group 1 Digital Input 2
11	I/O1 IRQ1	Interrupt pin for I/O group 1
12	EXT33	3.3 volt power supply
13	NC	Not connected

J701 – I/O Group 2 Connector:

Pin No	Name	Pin Description
1	VCC_5	5 volt power supply
2	VCC_5	5 volt power supply
3	GND	Ground
4	GND	Ground
5	RF2 RXD	Receiver (TTL level)
6	RF2 TXD	Transmitter (TTL level)
7	Digital O/P 2	Digital Output 2
8	Digital O/P 3	Digital Output 3
9	I/O 2 Digital I/P 1	I/O Group 2 Digital Input 1
10	I/O 2 Digital I/P 2	I/O Group 2 Digital Input 2
11	I/O2 IRQ	Interrupt pin for I/O Group 2
12	EXT33	3.3 volt power supply
13	NC	Not connected
14	NC	Not connected

J702- SPI Interface

Pin No	Name	Pin Description
1	SPICK	SPI clock
2	MISO	Master In Slave Out
3	MOSI	Master Out Slave In
4	$\overline{\text{CS}}$	Chip Select (Active low)
5	GND	Ground
6	NC	Not Connected

J200 – Debug Interface.

Pin No	Name	Pin Description
1	DBGU_TXD	Debug Transmitter (RS232 level)
2	GND	Ground
3	DBGU_RXD	Debug Receiver (RS232 level)

J300 – Opto Interface

Pin No	Name	Pin Description
1	OPTO 1 A	Optoisolator 1 Anode
2	OPTO 1 C	Optoisolator 1 Cathode
3	OPTO 2 A	Optoisolator 2 Anode

J301 – Opto+SSR interface

Pin No	Name	Pin Description
1	OPTO 2 C	Optoisolator 2 Cathode
2	EARTH	Earth
3	SSRRel2 +	SSR relay 1 +

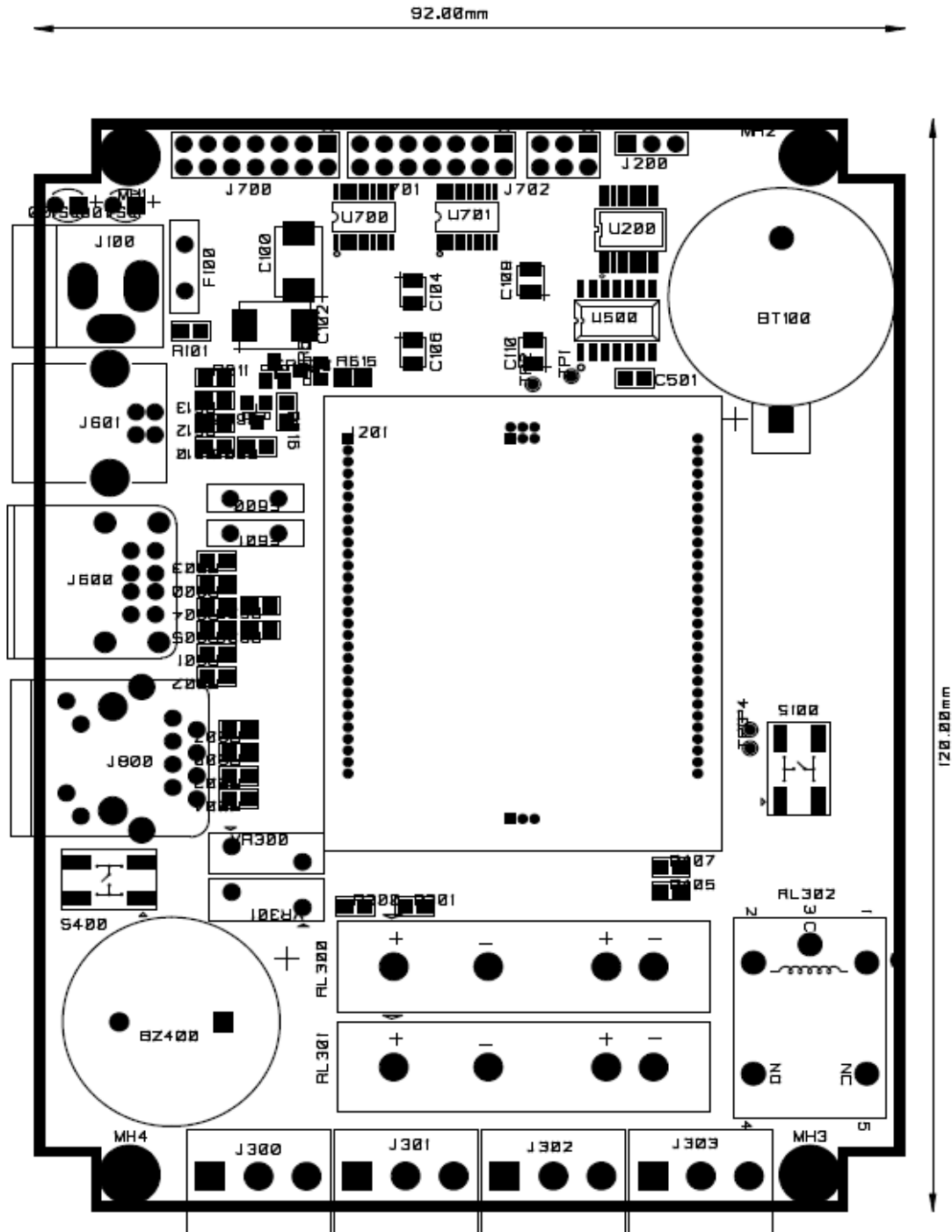
J302 – SSR interface

Pin No	Name	Pin Description
1	SSRRel2 -	SSR relay 1 -
2	SSRRel3 +	SSR relay 2 +
3	SSRRel3 -	SSR relay 2 -

J303 – SPDT interface

Pin No	Name	Pin Description
1	NO	Normally Open
2	COM	Common
3	NC	Normally close

### 3. Placement and Layout



## **4. Environmental**

Operating Temperature: **0 Degrees Celsius to + 50 Degrees Celsius**

## **5. Schematic**

**[Available on purchase of the board.](#)**