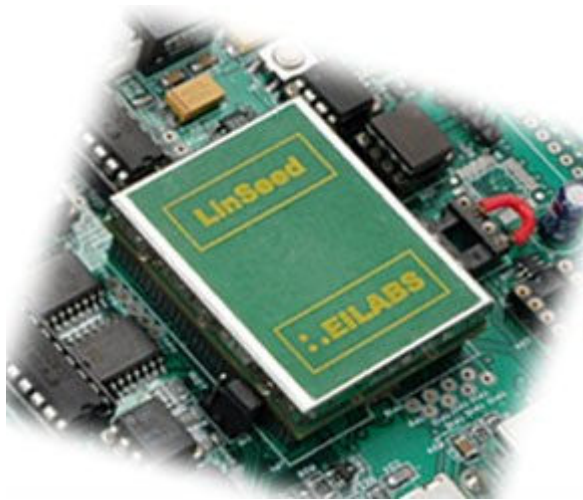


EI Labs India Pvt. Ltd.

Embedded Devices



# Application Controller With DPRAM

## Product Technical Information

Doc Name : Appln. Controller with DPRAM version 1.0

Dated : March 2008

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## 1. Overview

LinSeedV1 is a state of the art, 60 pin Integrated SoftChip and is the first in a series of LinSeed modules. The SoftChip concept encapsulates the hardware completely from a user perspective and provides them with a very high level software API for configuration, control and data processing. The LinSeedV1 is a 32 bit processing module with standard Linux API for the user. The hardware details are required only to the extent of the external interfaces on the user board for the purposes of further system development. Traditional SoC programming information like internal registers, peripherals etc are not required for the system designer of LinSeedV1. All peripherals are accessed through appropriate Linux drivers. This fundamentally is a big value proposition of the offering. Please refer the LinSeedV1 product technical information for more information.

Application Controller with DPRAM is built around LinSeedV1, and is USB and Ethernet enabled. It also has a 4K DPRAM, using which it can be used for communication with Legacy Processors and DSP's. This board can be used to acquire familiarity and expertise in handling the LinSeed module from the software development perspective, and interface it to Legacy Processors and legacy DSP's.

This Application controller board supports the following peripherals, features and Input/Outputs..

a.	USB 2.0 Full Speed Host Ports	2
b.	USB 2.0 Full Speed Device Port.	1
c.	4Kbyte DPRAM (15ns access time).	
d.	10 base T Ethernet (on SPI)	1
e.	Debug Port(RS232 Levels)	1

### **BLOCK DIAGRAM**

The block schematic of the Application Controller with DPRAM board is given in Figure 1.

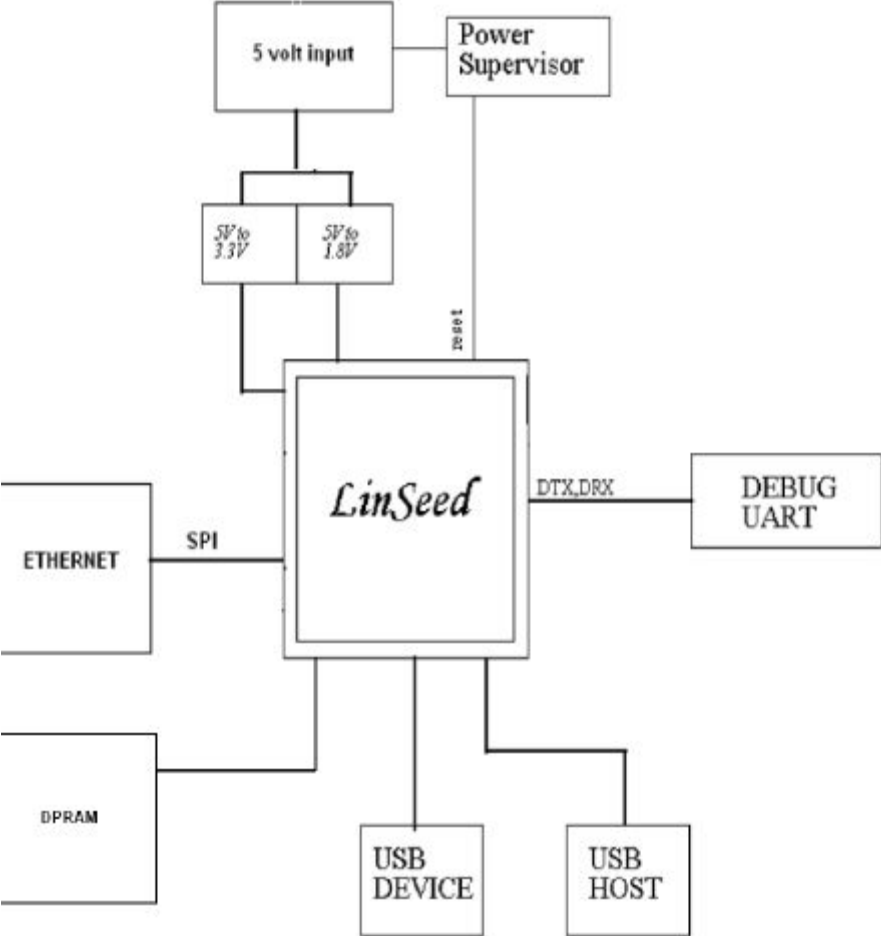


Figure 1 Application Controller with DPRAM functional block diagram

## 2. Functional Connector Pin Out

J304— USB Host: 2 Ports.

J303—USB Device: 1 port.

J305—Ethernet (10 Mbits/sec)

Pin No	Name	Pin Description
1	TX+	Ethernet TX+
2	TX-	Ethernet TX-
3	RX+	Ethernet RX+
6	RX_	Ethernet RX-
4		NC
5		NC
7		NC
8		NC
9	SHIELD	EARTH
10	SHIELD	EARTH
11	SHIELD	EARTH
12	SHIELD	EARTH

J302 – Debug RS232 Connector:

Debug UART pins are connected to this connector. All the signals are at RS232 level.

Pin No	Name	Pin Description
1	DBGU TXD	Debug Transmit Data
2	DBGU RXD	Debug Receive Data
3	GND	Ground

## JP500—(30X2, 60 pin External Interface)

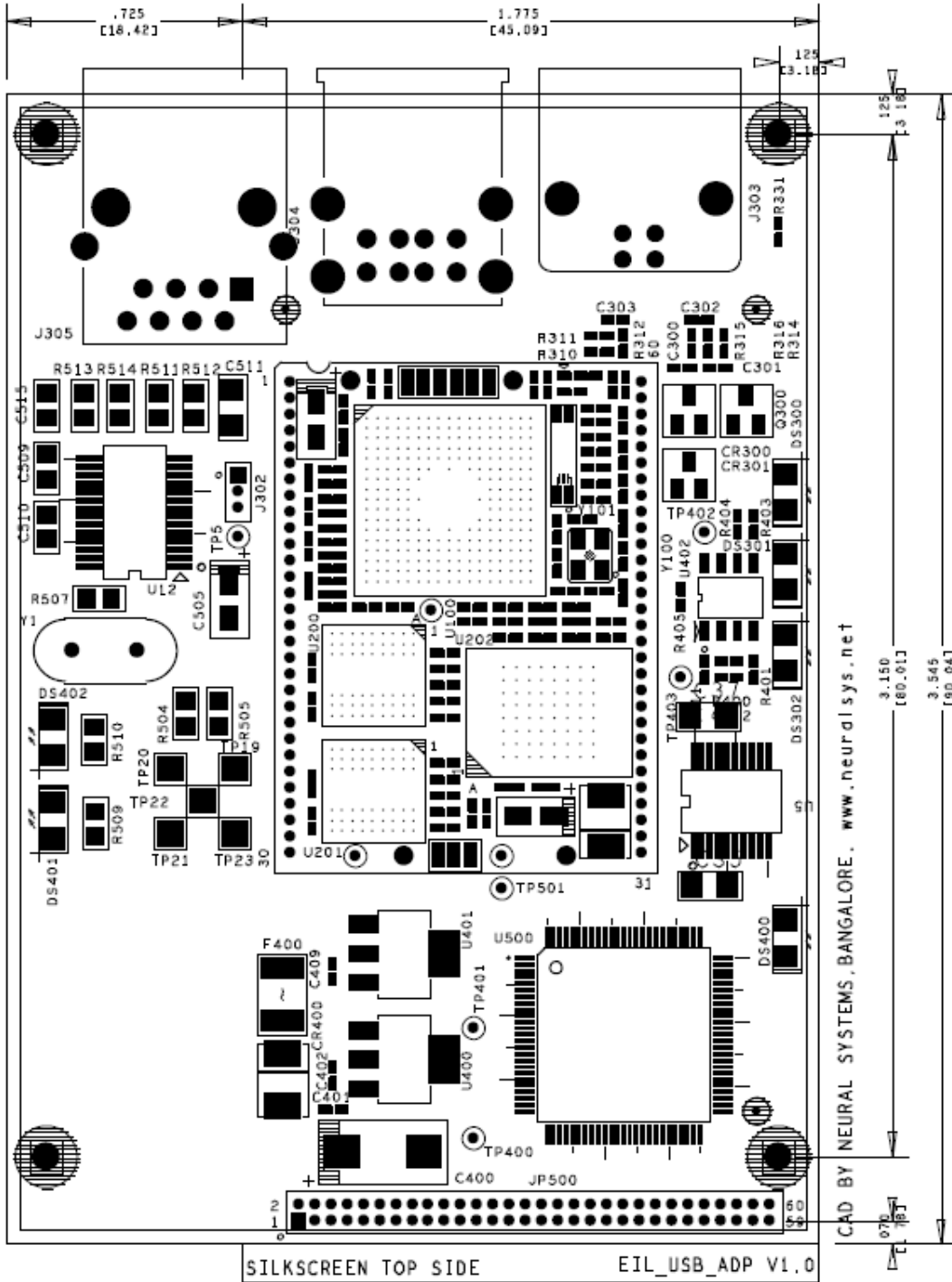
Pin No	Name	Pin Description
1	VCC_5	+5V DC Supply input
2	VCC_5	+5V DC Supply input
3	VCC_5	+5V DC Supply input
4	VCC_5	+5V DC Supply input
5	GND	Logic Ground
6	GND	Logic Ground
7	GND	Logic Ground
8	GND	Logic Ground
9	RA0	Address Bit 0(Right Port)
10	RD0	Data Bit 0(Right Port)
11	RA1	Address Bit 1(Right Port)
12	RD1	Data Bit 1(Right Port)
13	RA2	Address Bit 2(Right Port)
14	RD2	Data Bit 2(Right Port)
15	RA3	Address Bit 3(Right Port)
16	RD3	Data Bit 3(Right Port)
17	RA4	Address Bit 4(Right Port)
18	RD4	Data Bit 4(Right Port)
19	GND	Logic Ground
20	GND	Logic Ground
21	RA5	Address Bit 5(Right Port)
22	RD5	Data Bit 5(Right Port)
23	RA6	Address Bit 6(Right Port)
24	RD6	Data Bit 6(Right Port)
25	RA7	Address Bit 7(Right Port)
26	RD7	Data Bit 7(Right Port)
27	RA8	Address Bit 8(Right Port)
28	RD8	Data Bit 8(Right Port)
29	RA9	Address Bit 9(Right Port)
30	RD9	Data Bit 9(Right Port)

## Application Controller with DPRAM Product Technical Information

Pin No	Name	Pin Description
31	GND	Logic Ground
32	GND	Logic Ground
33	RA10	Address Bit 10(Right Port)
34	RD10	Data Bit 10(Right Port)
35	RA11	Address Bit 11(Right Port)
36	RD11	Data Bit 11(Right Port)
37	DPR_NCE	Chip Enable DPRAM
38	RD12	Data Bit 12(Right Port)
39	DPR_R/NW	H- Read , L-Write
40	RD13	Data Bit 13(Right Port)
41	DPR_NBUSY	Busy signal to DPRAM
42	RD14	Data Bit 14(Right Port)
43	NINT_IN	Interrupt from Legacy to core processor
44	RD15	Data Bit 14(Right Port)
45	VCC_5	+5V DC Supply input
46	DPR_NOE	Output Enable (DPRAM)
47	GND	Logic Ground
48	GND	Logic Ground
49	NINT_OUT	Interrupt from core processor to Legacy
50	VCC18	1.8V Supply Output
51	DPR_NSBM	Semaphore to DPRAM
52	H_STATUS	USB Host Port status
53	TXD	Debug port Transmit Data
54	D_STATUS	USB Device Port status
55	RXD	Debug port Receive Data
56	DPR_NINTR	DPRAM interrupt
57	VCC_5	+5V DC Supply input
58	NRST	Reset Signal (Active Low)
59	GND	Logic Ground
60	GND	Logic Ground

### 3. Placement and Layout.

Figure 2. Placement and Layout



## **4. Environmental**

Operating Temperature: **0 Degrees Celsius to + 50 Degrees Celsius**

## **5. Schematic**

[Available on purchase of the board.](#)